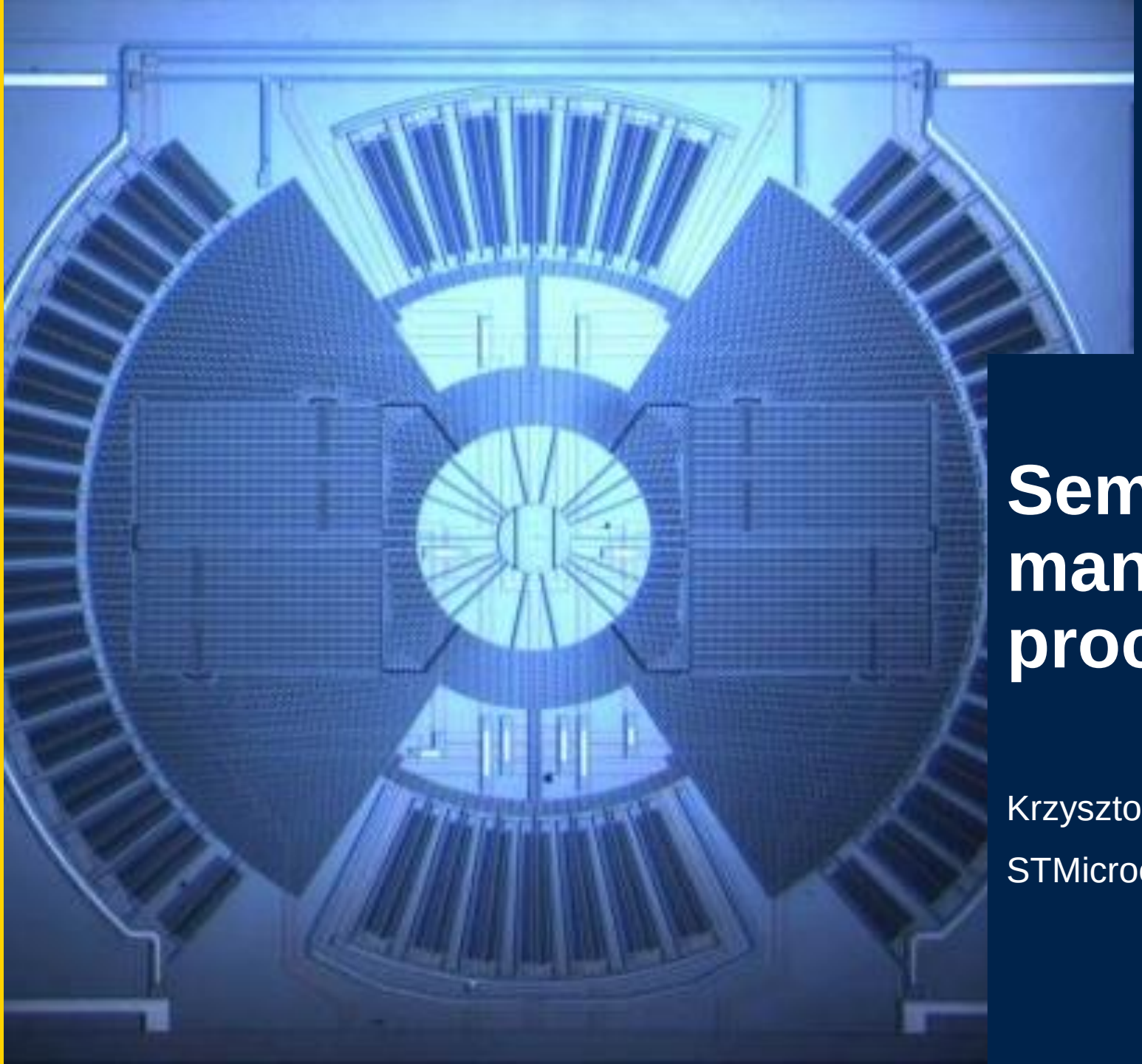

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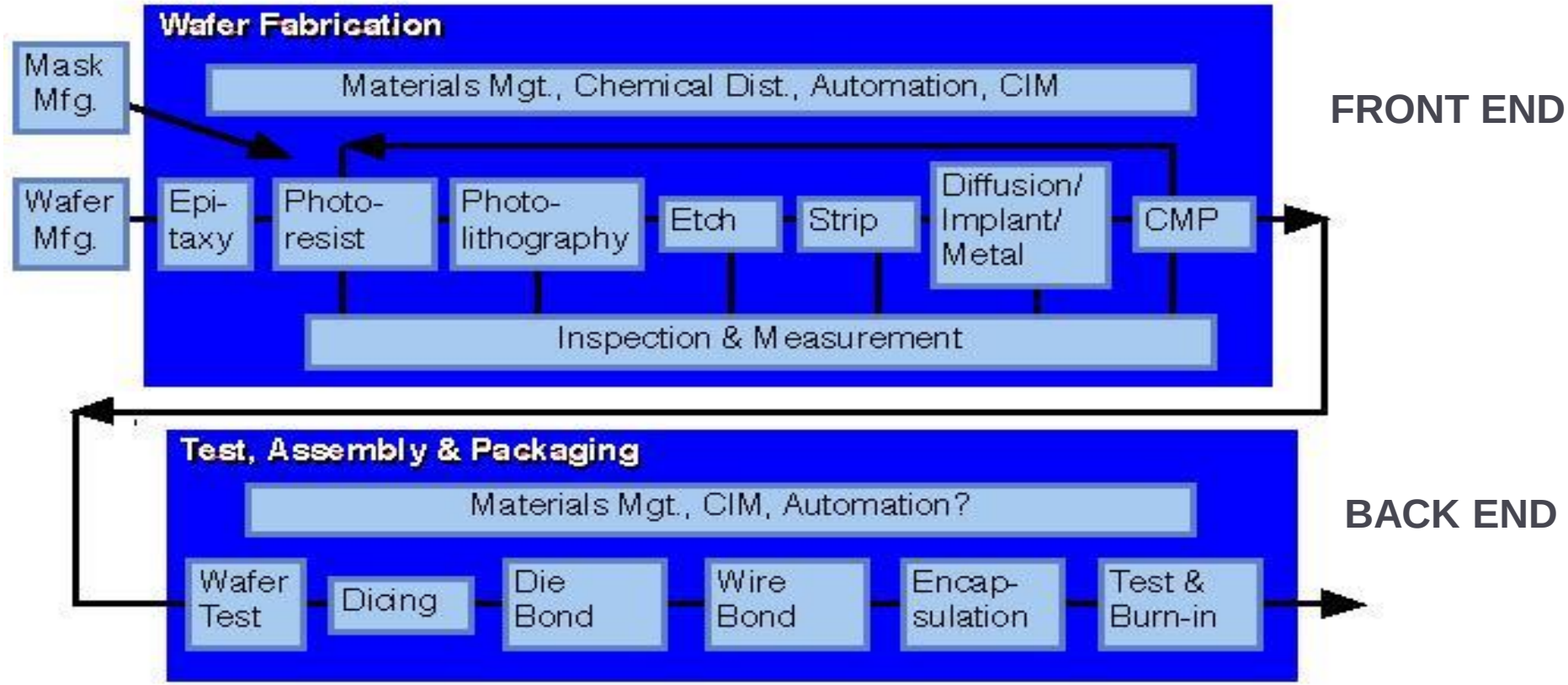
Semiconductors manufacturing process

Krzysztof Smolko

STMicroelectronics SA

Semiconductor manufacturing process



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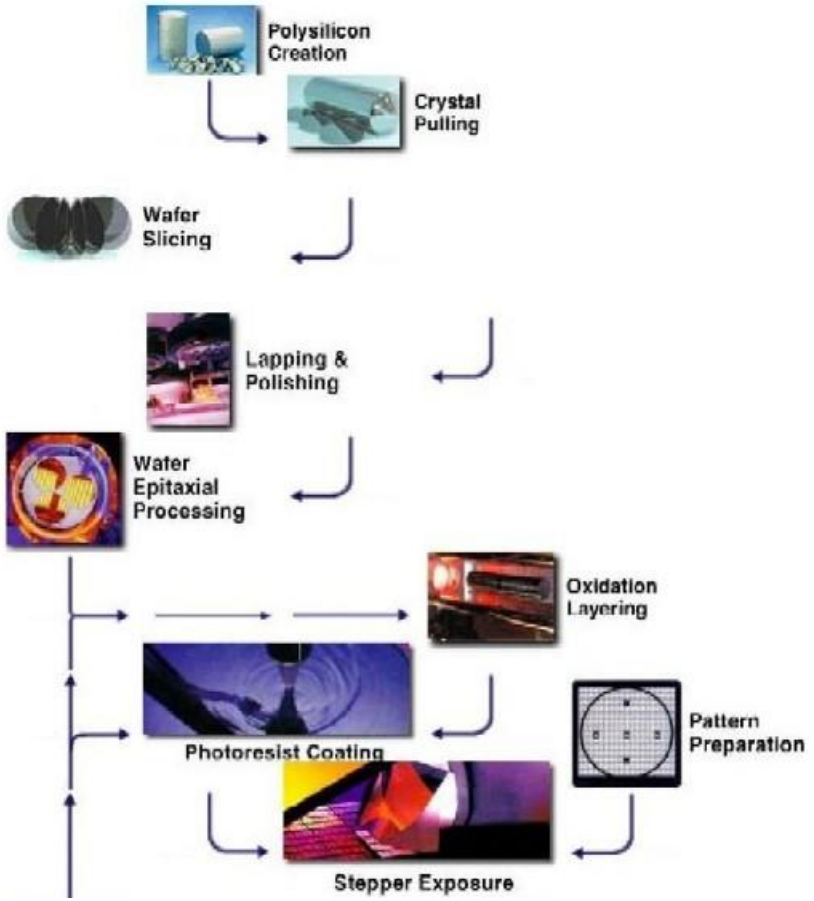
Semiconductor manufacturing process

Fundamental processing steps

1. Silicon manufacturing
   a) Czochralski method
   b) Wafer manufacturing
   c) Monocrystalline structure

2. Photolithography
   a) Photoresists
   b) Photomask and Reticles
   c) Patterning



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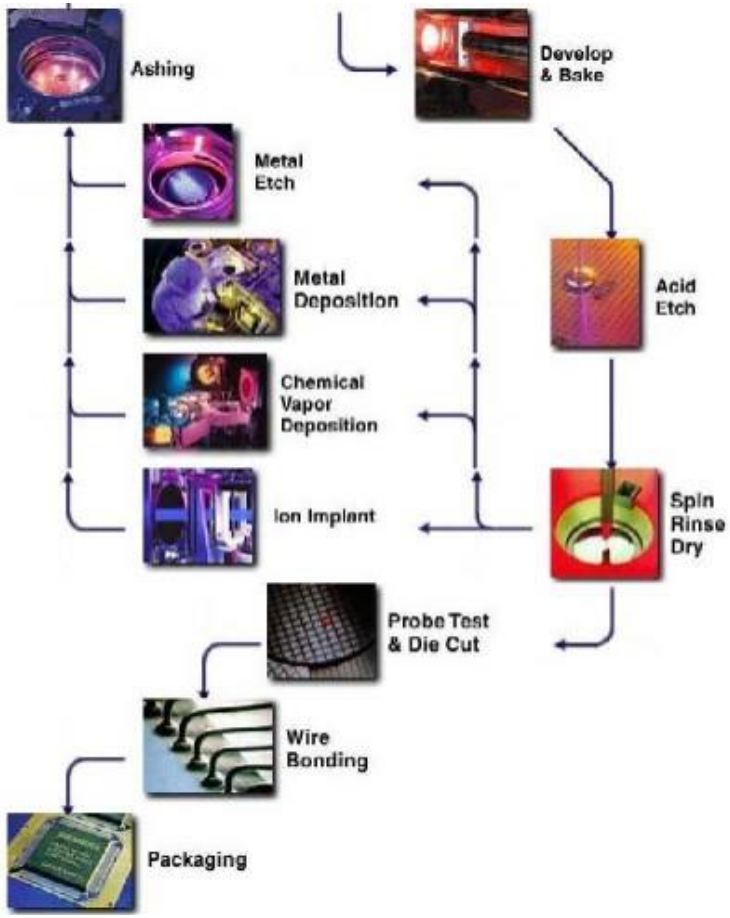
Semiconductor manufacturing process

Fundamental processing steps

3. Oxide growth & removal
   a) Oxide growth & deposition
   b) Oxide removal
   c) Other effects
   d) Local oxidation

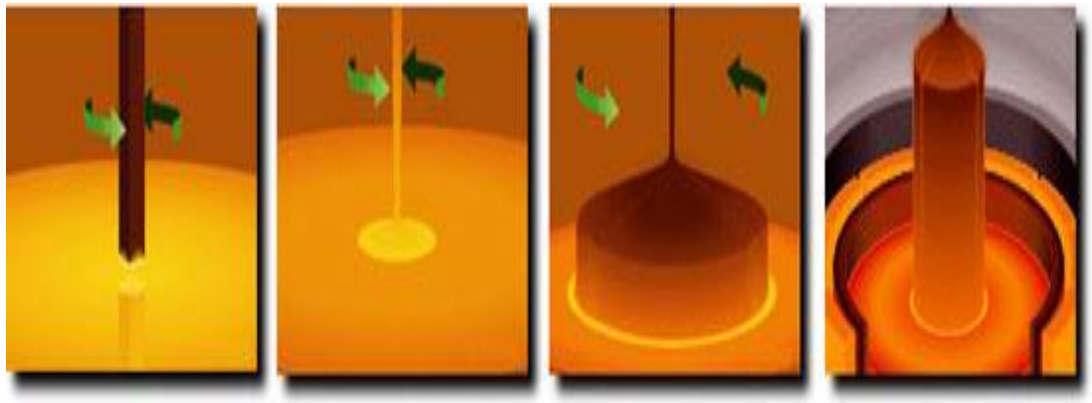
4. Diffusion & Ion implantation
   a) Diffusion
   b) Other effects
   c) Ion implantation

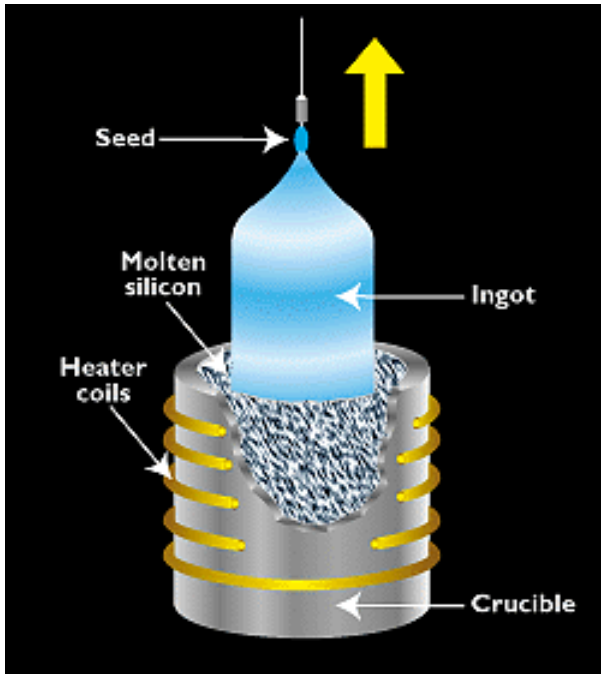


Crystal growth and wafer manufacturing

Crystal growth

- Czochralski Process is a technique of making monocrystalline silicon
- A solid seed crystal is rotated and slowly extracted from a pool of molten Si
- Requires careful control to give crystals desired purity and dimensions





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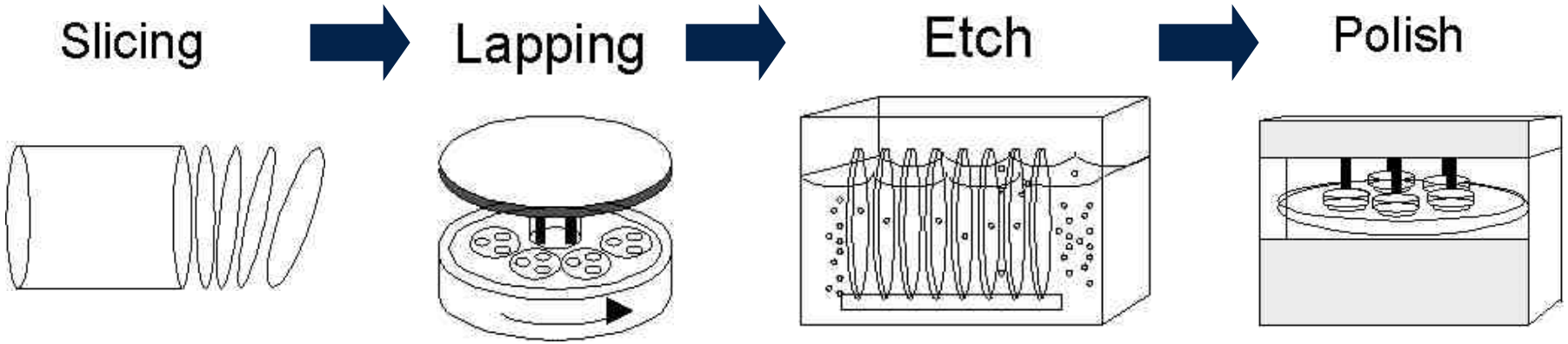
Cylinder of monocrystalline

- The silicon cylinder is known as an Ingot
- Typical Ingot is about 1 or 2 meters in length
- Can be sliced into hundreds of smaller circular pieces called Wafers
- Each Wafer yields hundreds or thousands of integrated circuits

Wafer manufacturing

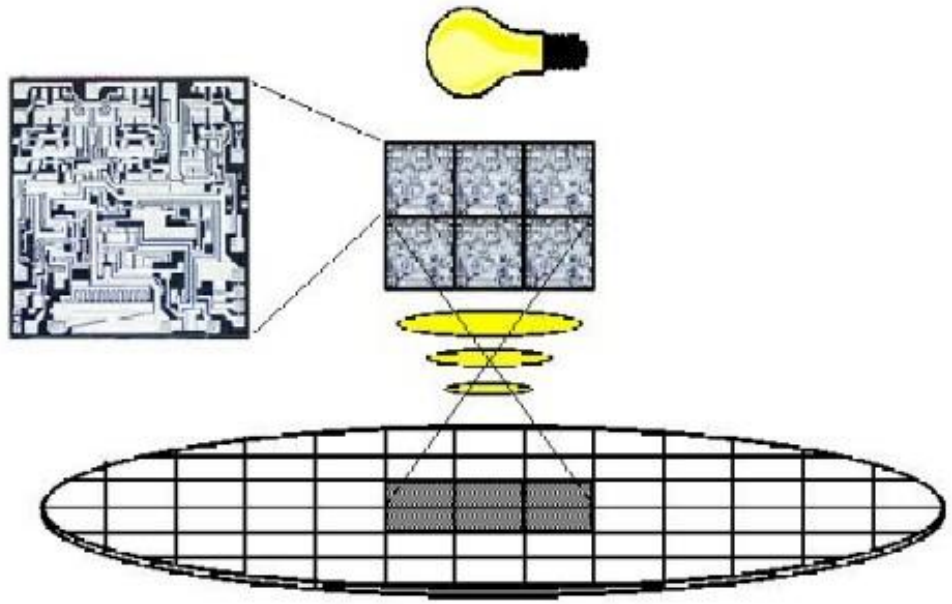
- The silicon crystal is sliced by using a diamond-tipped saw into thin wafers
- Sorted by thickness
- Damaged wafers removed during lapping
- Etch wafers in chemical to remove any remaining crystal damage
- Polishing flattens uneven surface left by sawing process



Photolithography

Photolithography

Photolithography is a technique that is used to define the shape of micro-machined structures on a wafer.



Photolithography
Photoresist

The first step in the photolithography process is to develop a mask, which will be typically a chromium pattern on a glass plate.

Next, the wafer is then coated with a polymer which is sensitive to ultraviolet light called a photoresist.

Afterward, the photoresist is then developed which transfers the pattern on the mask to the photoresist layer.

Photolithography
Photoresist

There are two basic types of photoresists.

Positive resists.

Positive resists are decomposed with ultraviolet light. The resist is exposed to UV light wherever the underlying material has to be removed. In these resists, exposure to the UV light changes the chemical structure of the resist so that it becomes more soluble in the developer. The exposed resist is then washed-away by the developer solution, leaving windows of the bare underlying material. The mask, therefore, contains an exact copy of the pattern which is to remain on the wafer

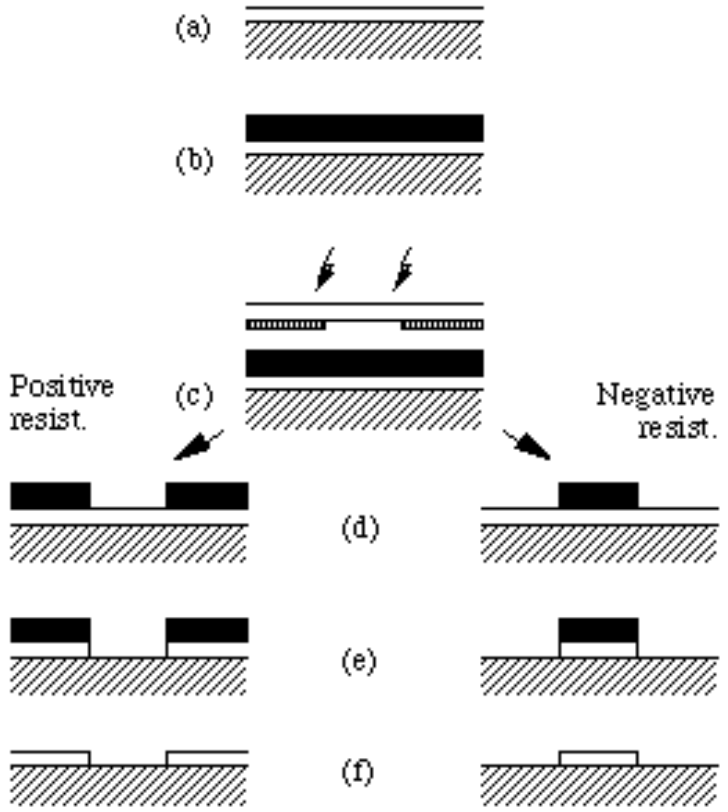
Photolithography
Photoresist

Negative resists

Exposure to the UV light causes the negative resist to become polymerized, and more difficult to dissolve. Therefore, the negative resist remains on the surface wherever it is exposed, and the developer solution removes only the unexposed portions. Masks used for negative photoresists, therefore, contain the inverse (or photographic "negative") of the pattern to be transferred.

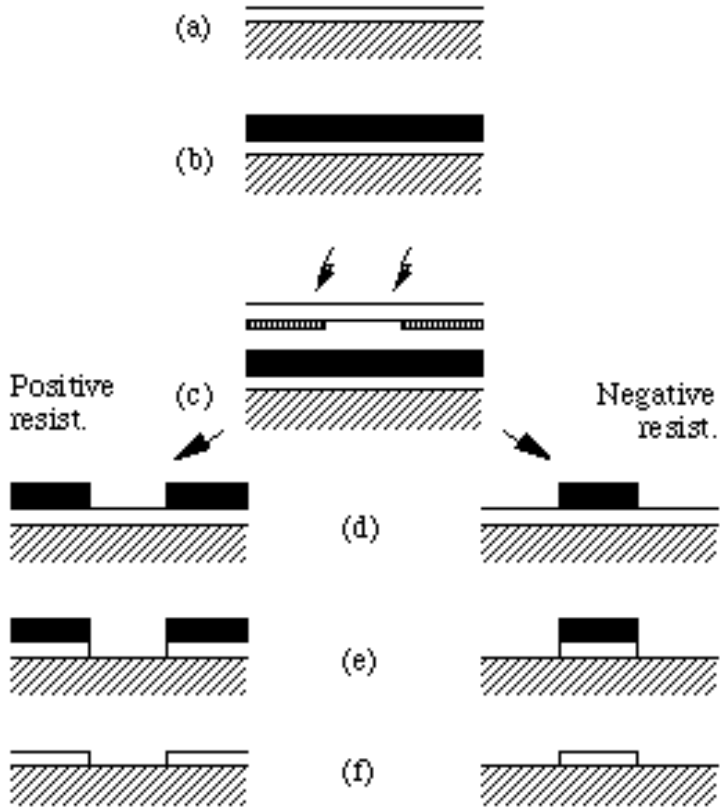
Photolithography Model

- Figure **a** shows a thin film of some material (i.e. silicon dioxide) on a substrate of some other material (i.e. a silicon wafer).
- Photoresist layer (figure **b**)
- Ultraviolet light is then shone through the mask onto the photoresist (figure **c**).



Photolithography Model

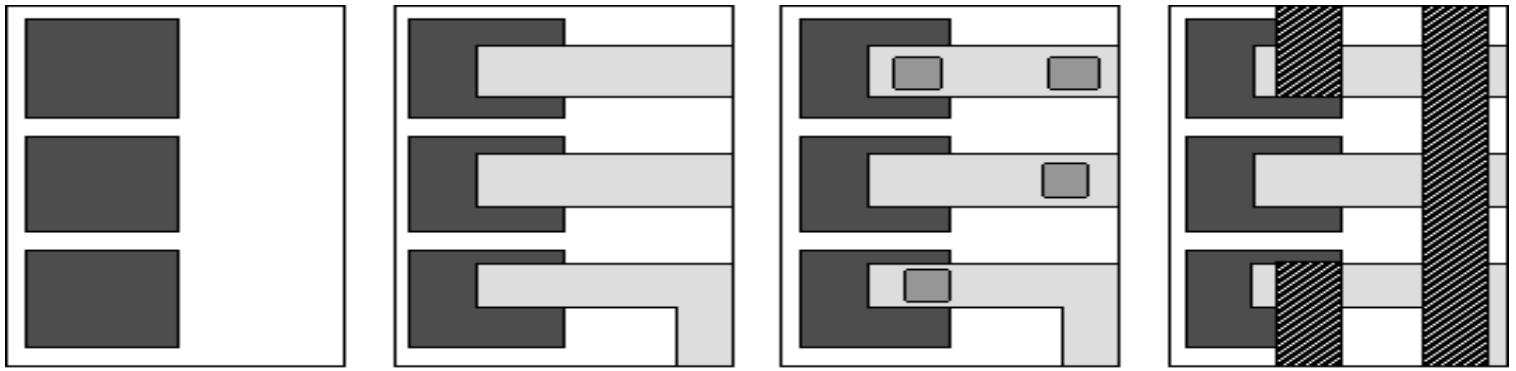
- The photoresist is then developed which transfers the pattern on the mask to the photoresist layer (figure **d**).
- A chemical (or some other) method is then used to remove the oxide where it is exposed through the openings in the resist (figure **e**).
- Finally, the resist is removed leaving the patterned oxide (figure **f**).



Photolithography
Photomasks and Reticles

Photomask

This is a square glass plate with a patterned emulsion of metal film on one side. The mask is aligned with the wafer, so that the pattern can be transferred onto the wafer surface. Each mask after the first one must be aligned to the previous pattern.



Photolithography
Photomasks and Reticles

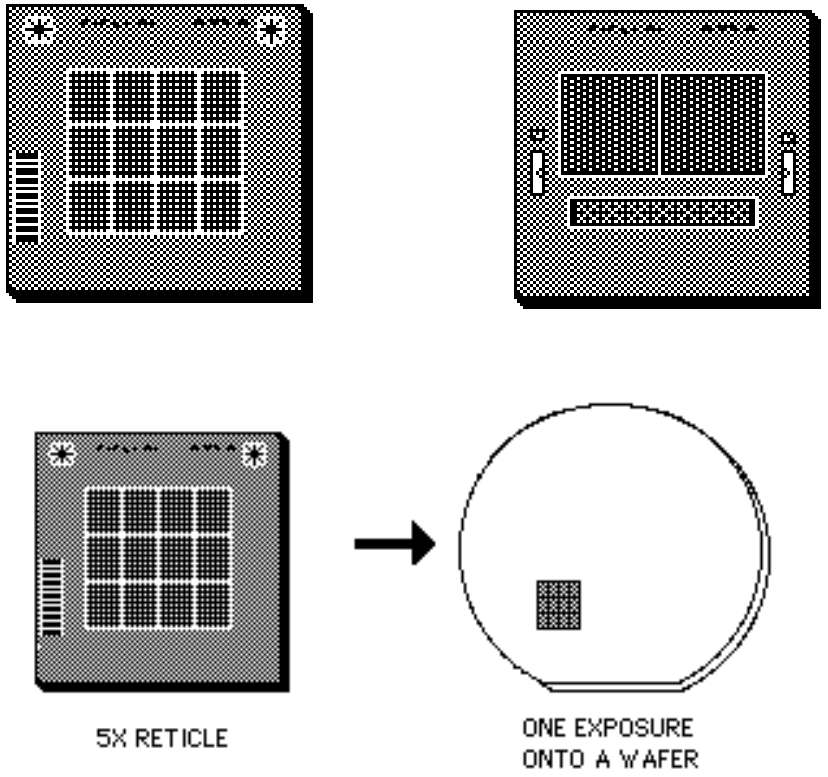
When an image on the photomask is projected several times side by side onto the wafer, this is known as **stepping** and the photomask is called a **reticle**.

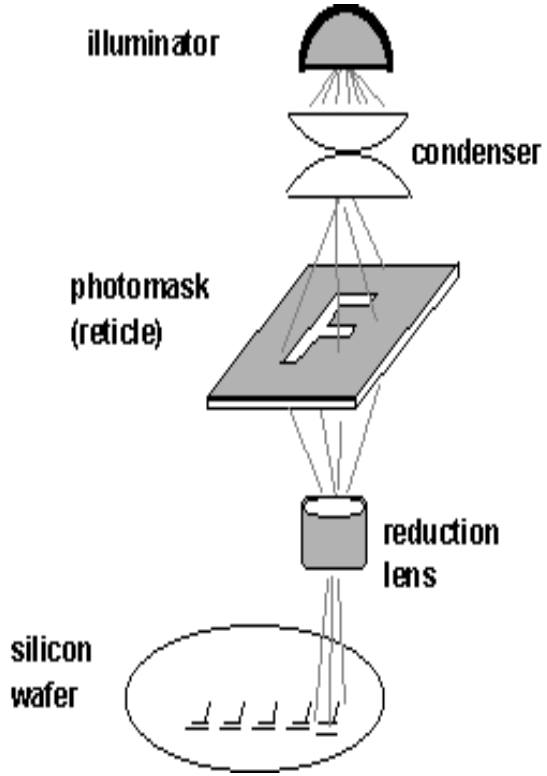
A common reticle is the 5X

The patterns on the 5X reticle are reduced 5 times when projected onto the wafer. This means the dies on the photomask are 5 times larger than they are on the final product. There are other kinds of reduction reticles (2X, 4X, and 10X), but the 5X is the most commonly used. Reduction reticles are used on a variety of steppers, the most common being ASM, Canon, Nikon, and GCA.

Photolithography
Photomasks and Reticles

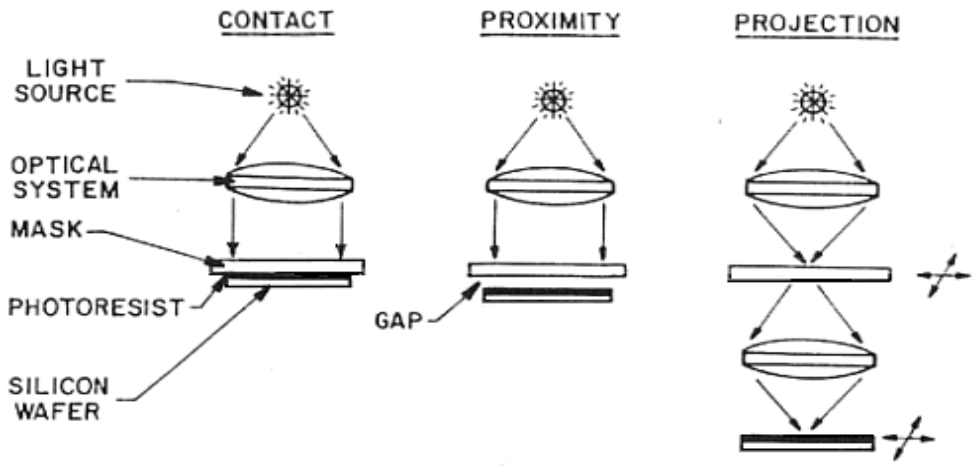
Examples of 5X Reticles:





Photolithography
Photomasks and Reticles

Once the mask has been accurately aligned with the pattern on the wafer's surface, the photoresist is exposed through the pattern on the mask with a high intensity ultraviolet light. There are three primary exposure methods: contact, proximity, and projection.



Photolithography Patterning

The last stage of Photolithography is a process called **ashing**. This process has the exposed wafers sprayed with a mixture of organic solvents that dissolves portions of the photoresist .

Conventional methods of **ashing** require an oxygen-plasma ash, often in combination with halogen gases, to penetrate the crust and remove the photoresist. Usually, the plasma **ashing** process also requires a follow-up cleaning with wet-chemicals and acids to remove the residues and non-volatile contaminants that remain after **ashing**. Despite this treatment, it is not unusual to repeat the "ash plus wet-clean" cycle in order to completely remove all photoresist and residues.

Oxidation of Silicon

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Oxidation of Silicon

- SiO_2 growth is a key process step in manufacturing all Si devices

- Thick (1μm) oxides are used for field oxides (isolate devices from each other)

- Thin gate oxides (100 Å) control MOS devices

- Sacrificial layers are grown and removed to clean-up surfaces

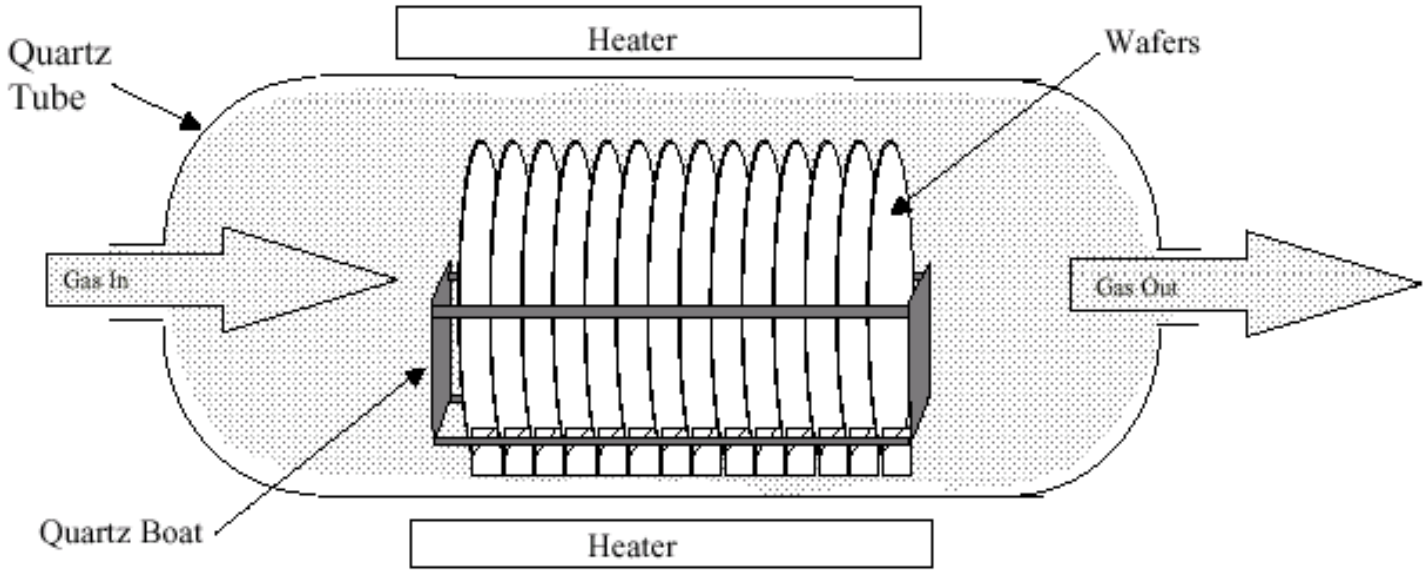
- The stability and ease of formation of SiO_2 was one of the reasons that Si replaced Ge as the semiconductor of choice.

Oxidation of Silicon

The simplest method of producing an oxide layer consists of heating a silicon wafer in an oxidizing atmosphere.

- Heat wafers in an atmosphere containing an oxidant, usually O_2, steam, or N_2O.

$$Si + O_2 \rightarrow SiO_2$$
$$Si + 2H_2O \rightarrow SiO_2 + 2H_2$$
$$Si + 2N_2O \rightarrow SiO_2 + 2N_2$$



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Oxidation of Silicon

- **Dry oxide -** Pure dry oxygen is employed

Disadvantage

- Dry oxide grows very slowly.

Advantage

- Oxide layers are very uniform.
- Relatively few defects exist at the oxide-silicon interface (These defects interfere with the proper operation of semiconductor devices)
- It has especially low surface state charges and thus make ideal dielectrics for MOS transistors.

Oxidation of Silicon

- **Wet oxide -** In the same way as dry oxides, but steam is injected

Disadvantage

- Hydrogen atoms liberated by the decomposition of the water molecules produce imperfections that may degrade the oxide quality.

Advantage

- Wet oxide grows fast.
- Useful to grow a thick layer of field oxide

Deposited Oxides

- Oxide is frequently employed as an insulator between two layers of metallization. In such cases, some form of **deposited oxide** must be used rather than the grown oxides.
- Deposited oxides can be produced by various reactions between gaseous silicon compounds and gaseous oxidizers. Deposited oxides tend to possess low densities and large numbers of defect sites. Not suitable for use as gate dielectrics for MOS transistors but still acceptable for use as insulating layers between multiple conductor layers, or as protective overcoats.

Key Variables in Oxidation

- **Temperature**
  - reaction rate
  - solid state diffusion
- **Oxidizing species**
  - wet oxidation is much faster than dry oxidation
- **Surface cleanliness**
  - metallic contamination can catalyze reaction
  - quality of oxide grown (interface states)

Etching

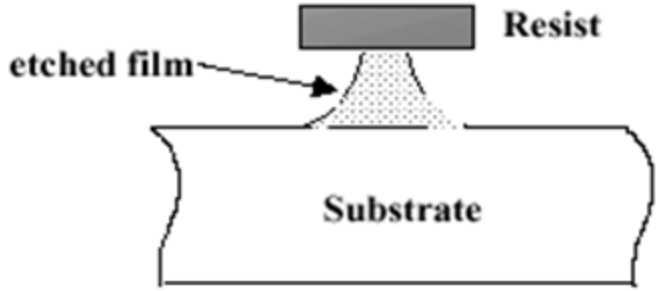
Etching is the process where unwanted areas of films are removed by either dissolving them in a wet chemical solution (**Wet Etching**) or by reacting them with gases in a plasma to form volatile products (**Dry Etching**).

Resist protects areas which are to remain. In some cases a hard mask, usually patterned layers of SiO_2 or Si_3N_4, are used when the etch selectivity to photoresist is low or the etching environment causes resist to delaminate.

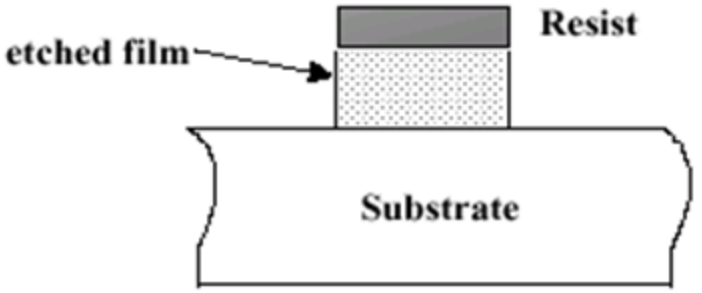
This is part of lithography - pattern transfer.

Etching Terminology

- **Isotropic etch**
  - a process that etches at the same rate in all directions.



- **Anisotropic etch**
  - a process that etches only in one direction.



Wet Chemical Etching

- **Wet etches**:
  - are in general isotropic (not used to etch features less than ≈ 3 μm)
  - achieve high selectivity for most film combinations
  - capable of high throughputs
  - use comparably cheap equipment
  - can have resist adhesion problems
  - can etch just about anything

Example Wet Processes

- **For SiO_2 etching**
  - $HF + NH_4F + H_20$ (buffered oxide etch or BOE)

- **For Si_3N_4**
  - Hot phosphoric acid: H_3PO_4 at 180 °C
  - need to use oxide hard mask

- **Silicon**
  - Nitric, HF, acetic acids
  - $HNO_3 + HF + CH_3COOH + H_2O$

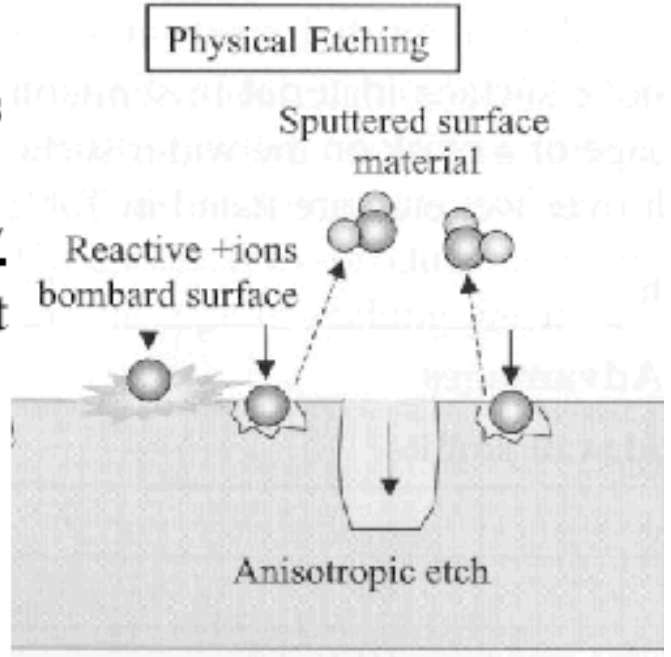
- **Aluminum**
  - Acetic, nitric, phosphoric acids at 35-45 °C
  - $CH_3COOH + HNO_3 + H_3PO_4$

What is a plasma (glow discharge)?

- A plasma is a partially ionized gas made up of equal parts positively and negatively charged particles.
- Plasmas are generated by flowing gases through an electric or magnetic field.
- These fields remove electrons from some of the gas molecules.
  The liberated electrons are accelerated, or energized, by the fields.
- The energetic electrons slam into other gas molecules, liberating more electrons, which are accelerated and liberate more electrons from gas molecules, thus sustaining the plasma.

Dry or Plasma Etching

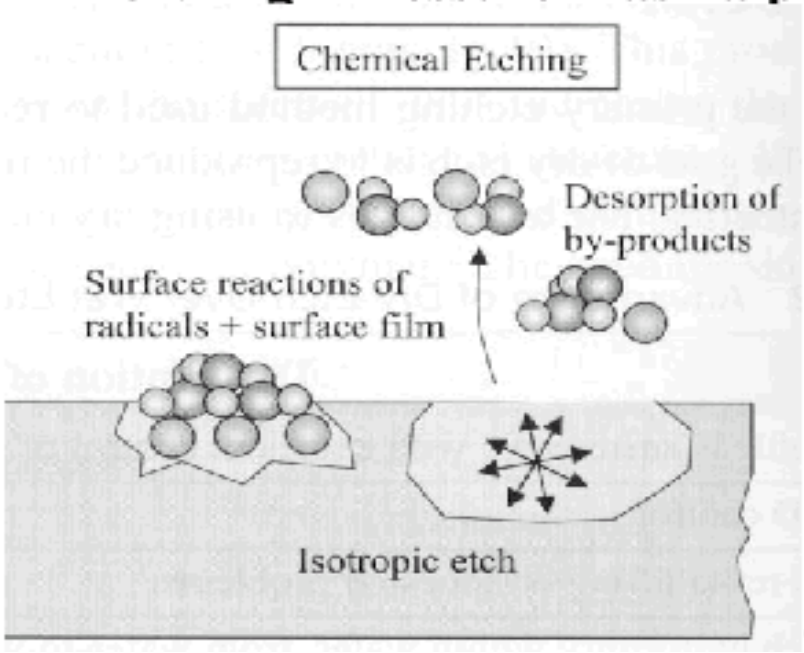
- **Three different mechanisms**
  - **Purely physical (sputtering)**
    - **Can be anisotropic**
    - **All materials have sputter yields within a factor of about 3, therefore selectivities will be low**
    - **nonvolatile species can redeposit on surfaces**
    - **ex. Ion Milling process**



Semiconductor Manufacturing Technology, Quirk and Serda, Prentice Hall,2001

Dry or Plasma Etching

- **Purely chemical**
  - **isotropic**
  - **can have high selectivities**
  - **similar to wet etching**
  - **ex. High Pressure Plasma process**



Semiconductor Manufacturing Technology, Quirk and Serda, Prentice Hall,2001

Dry or Plasma Etching

Combination of chemical and physical etching

Reactive Ion Etching (RIE)

Directional etching due to ion assistance.

In RIE processes the wafers sit on the powered electrode. This placement sets up a negative bias on the wafer which accelerates positively charge ions toward the surface.

These ions enhance the chemical etching mechanisms and allow **anisotropic** etching.

Wet etches are simpler, but **dry etches** provide better line width control since it is anisotropic.

Other Effects of Oxide Growth and Removal

- Oxide Step
  - The differences in oxide thickness and in the depths of the silicon surfaces combine to produce a characteristic surface discontinuity
- The growth of a thermal oxide affects the doping levels in the underlying silicon
- The doping of silicon affects the rate of oxide growth

Local Oxidation of Silicon (LOCOS)

- LOCOS: localized oxidation of silicon using silicon nitride as a mask against thermal oxidation.
- A technique called local oxidation of silicon (LOCOS) allows the selective growth thick oxide layers
- CMOS and BiCMOS processes employ LOCOS to grow a thick field oxide over electrically inactive regions of the wafer

Diffusion and Ion Implantation

PN-Junction Fabrication (Earliest method)

- **Process:**
  - Opposite polarity doping atoms are added to molten silicon during the *Czochralski process* to create in-grown junctions in the ingot.
  - Repeated counter-doping can produce multiple junctions within the crystal.
- **Disadvantages**
  - Inability to produce differently doped areas in different parts of the wafer.
  - The thickness and planarity of grown junctions are difficult to control.
  - Repeated counter-doping degrade the electrical properties of the silicon.

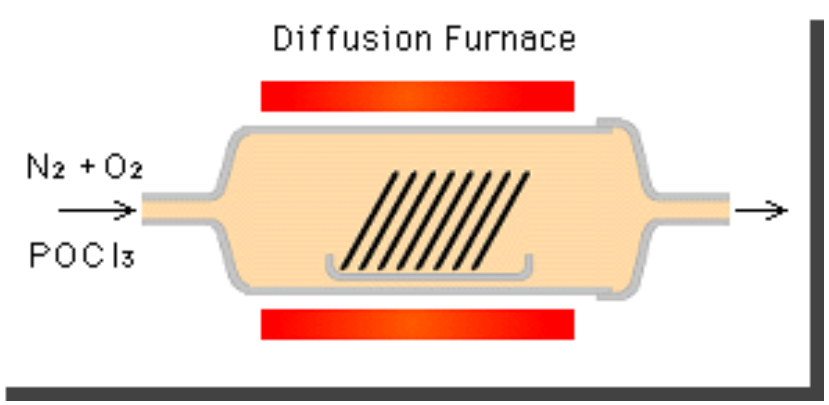
Planar process

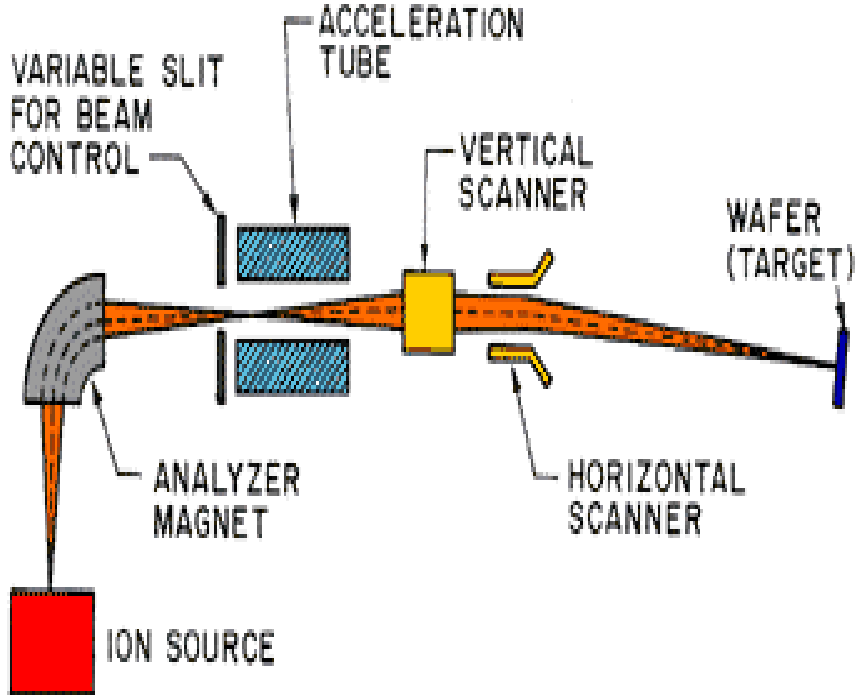
- **Advantages**:
  - The planar process does not require multiple counter-doping of the silicon ingot.
  - This process allows more precise control of junction depths and dopant distributions.

Methods of Planar process

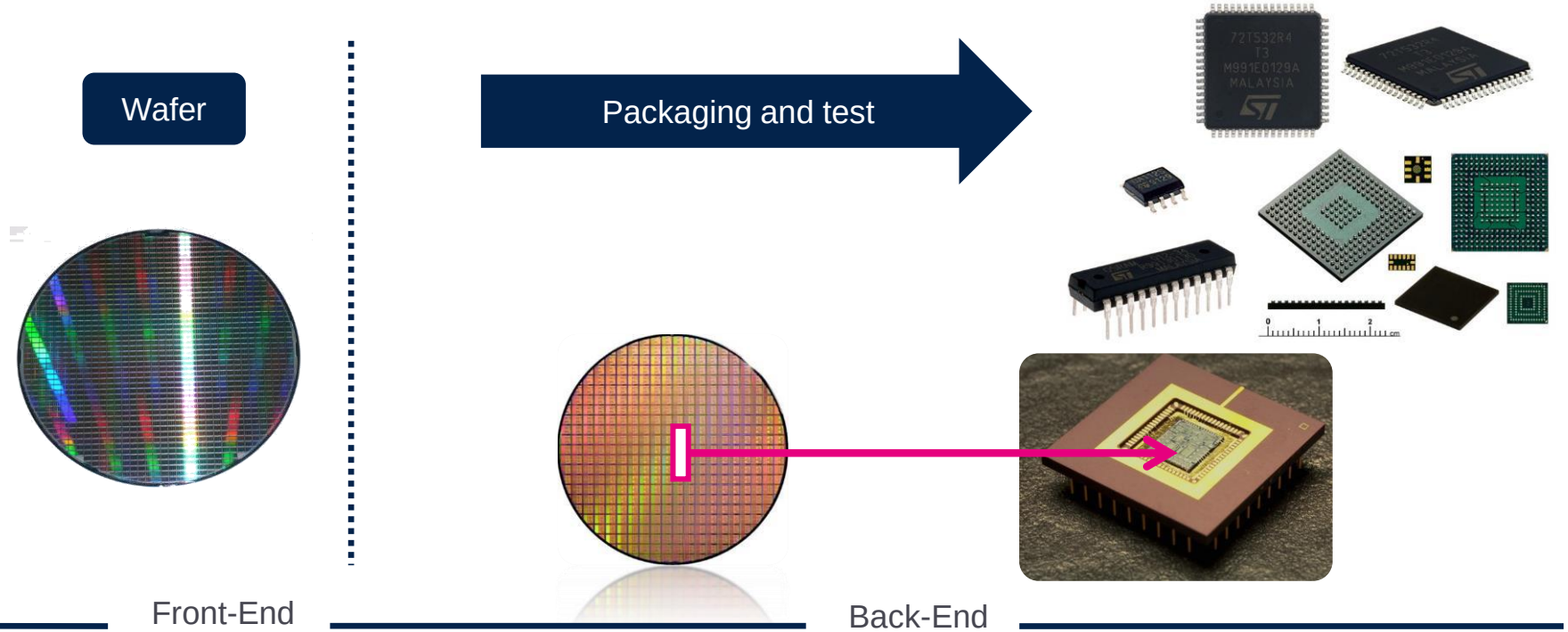
- **Diffusion**
  - A uniformly doped ingot is sliced into wafers.
  - An oxide film is then grown on the wafers.
  - The film is patterned and etched using photolithography exposing specific sections of the silicon.
  - The wafers are then spun with an opposite polarity doping source adhering only to the exposed areas.
  - The wafers are then heated in a furnace (800-1250C) to drive the doping atoms into the silicon.
- **Ion Implantation**
  - A particle accelerator is used to accelerate a doping atom so that it can penetrate a silicon crystal to a depth of several microns
  - Lattice damage to the crystal is then repaired by heating the wafer at a moderate temperature for a few minutes. This process is called annealing.

Diffusion Process
Ion Implantation





From silicon wafer to final components



A unit of wafer, known as a “die”, is used to make a single semiconductor device
Packaging provides the protection and the interconnection from the circuit to the printed circuit board for the final application

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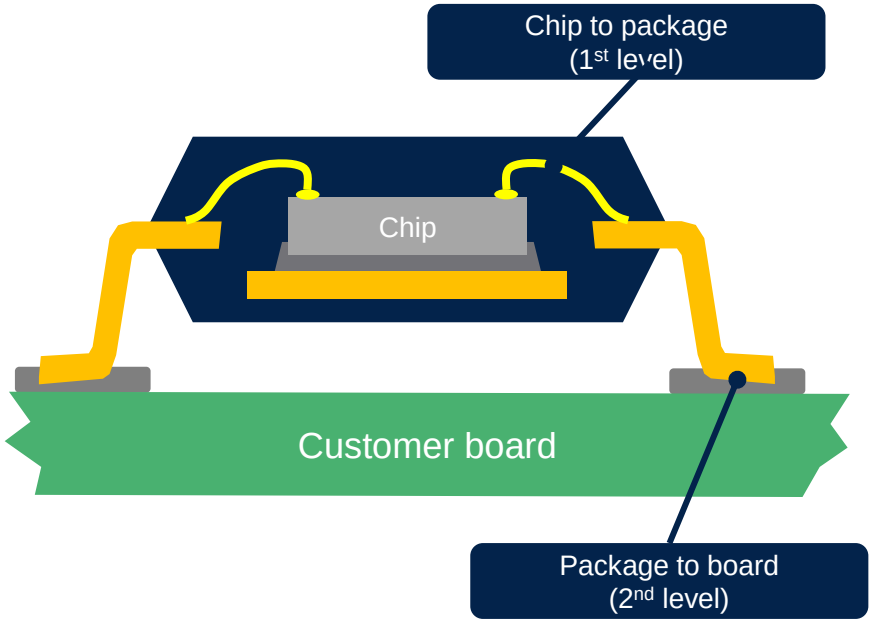
What is a package?

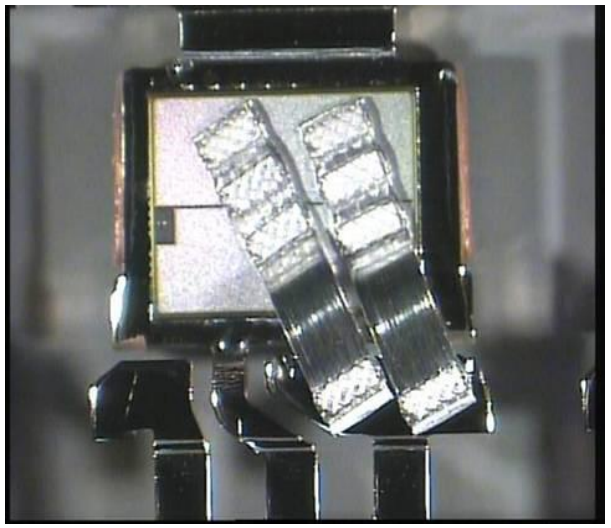


Package links chip with customer boards

- Mechanical
  - Protection of chip layers
  - Standardized outline and footprint
- Electrical
  - Electrical path chip to board
  - Signal integrity
- Thermal
  - Conduct heat to the “outside”
  - Keep temperature junction within range

What is a package?

wires

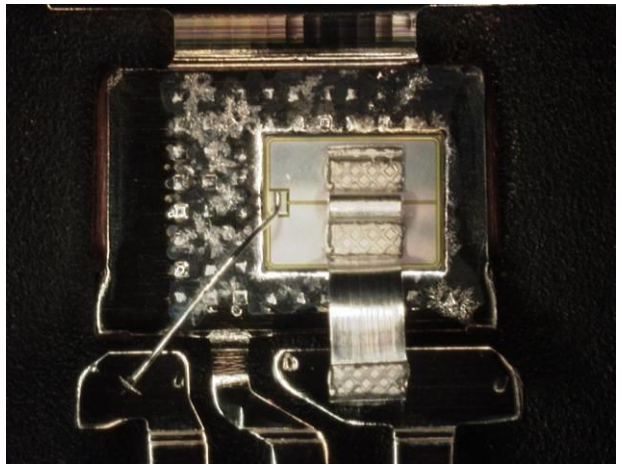


ribbons

From *Wires* to *Ribbons*:

- Higher current capacity due to the bigger equivalent area
- Lower mechanical stress during bonding
- Improved Rdson due to the lower contact's resistance
- Same process (ultrasonic wire bonding) and materials (Al 99.99)

What is a package?



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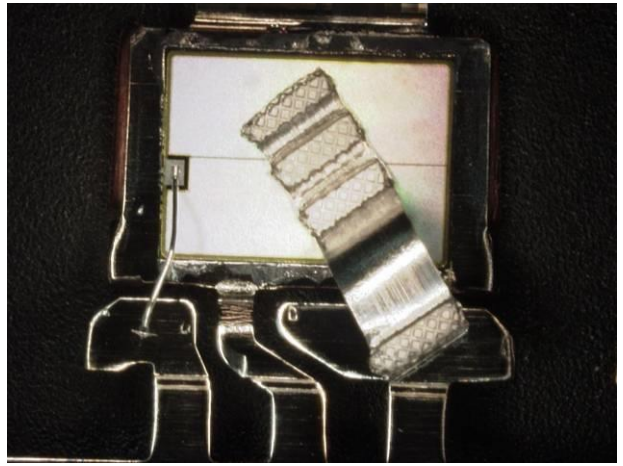

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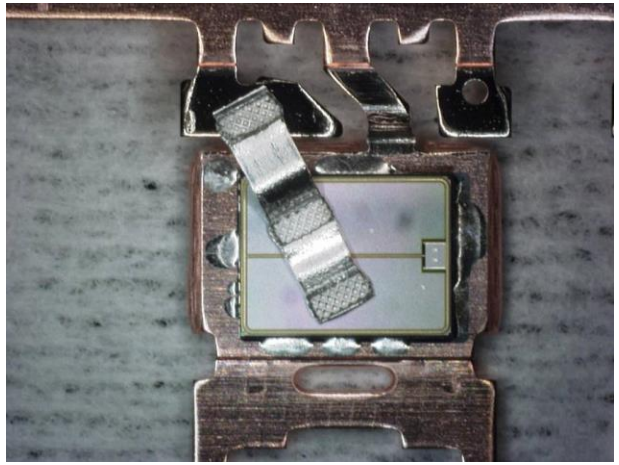
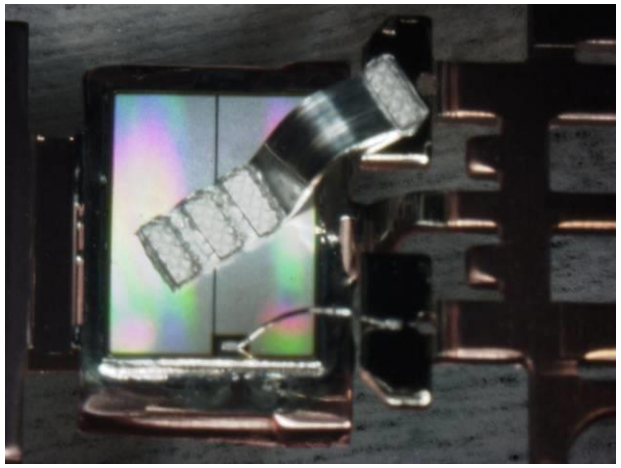


DPAK



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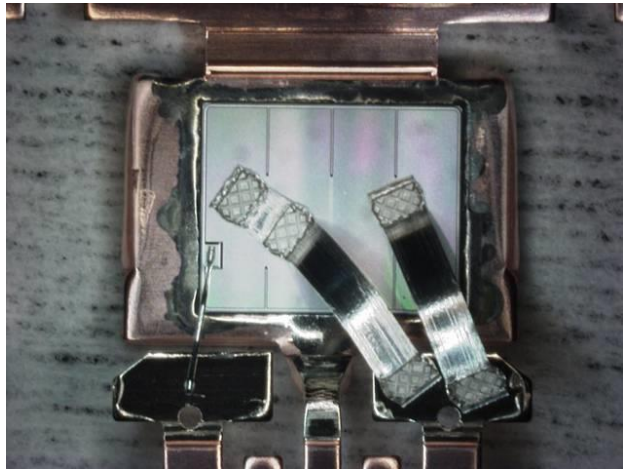

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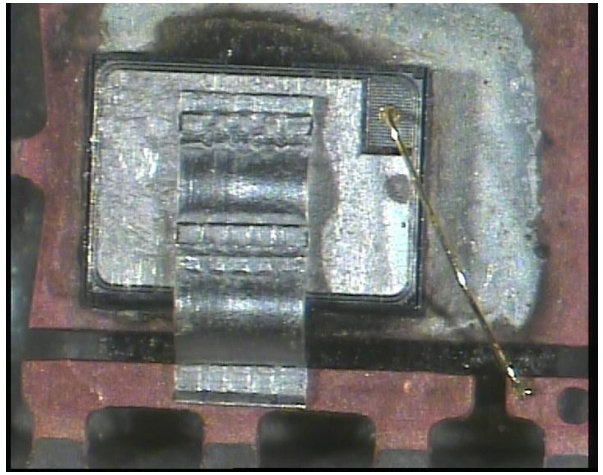

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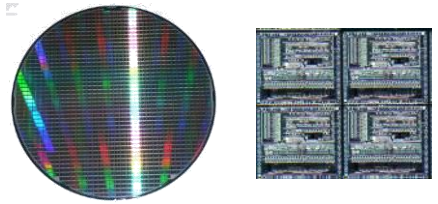
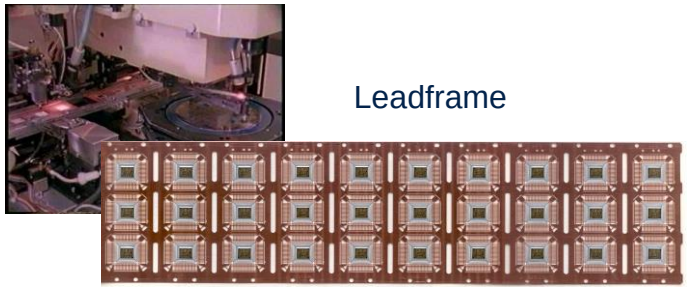
Back End key manufacturing steps

Wafer saw – Die attach – Wire bonding - Molding

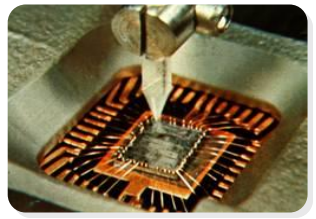


Wafer saw:
The wafer is cut into individual dice

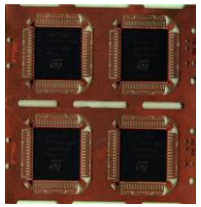


Leadframe

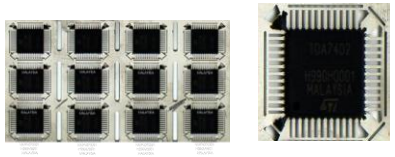
Die attach:
Dice are assembled on a leadframe – this will be the “legs” of the final component



Wire bond:
The “legs” of the lead frame are connected via gold / copper wires to the bond pads on the chip



Molding / Encapsulation:
The plastic body of the microchip is molded around the die and partially over the leadframe



Laser marking:
The corporate and product identification (plant name, ST logo) are placed on the packaged device.

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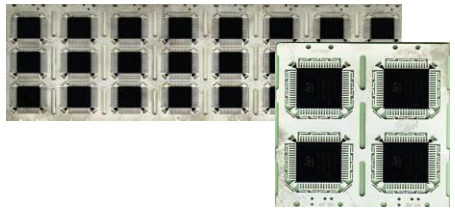
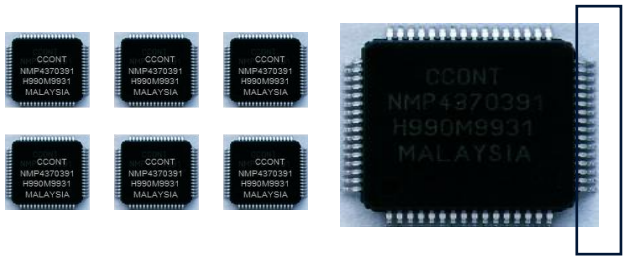
Back End key manufacturing steps

Plating – Trim & Form – Testing - Finishing

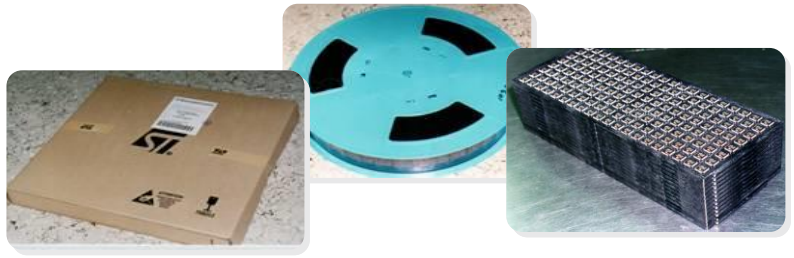


Plating:
A thin layer of solder material is deposited on the leadframe



Trim & form:
Individual leads of the leadframe are separated and formed to a specified shape

Testing:
The functionality of each unit is verified through an automatic sequence of electrical tests



Mechanical inspection and packing
External visual inspection and packing material to be sent to warehouse as finished goods

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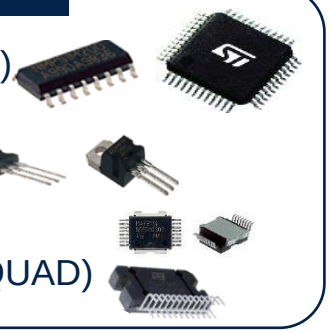
PTM package portfolio

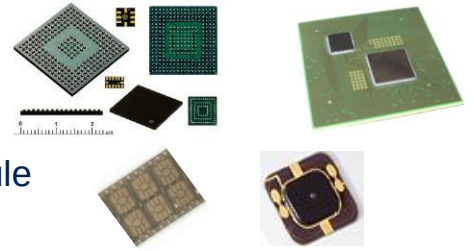
Leadframe

- Signal package (SO, QFP, QFN)
- Power discrete (TO2XX)
- Power SMDs (PSO, PSSO, HiQUAD)



Laminate

- BGA
- Micromodule



Sensor Package

- MEMS
- Proximity sensor

Wafer Level Package

- Wafer Level Package

More than 750 package references enabling ST product groups

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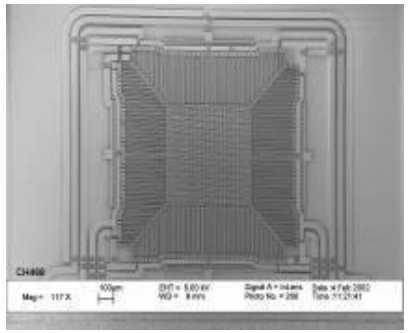
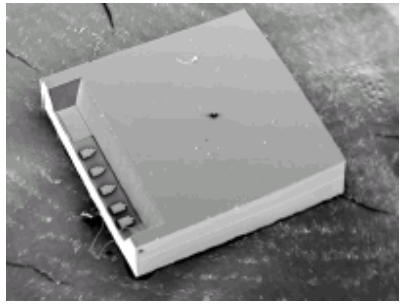
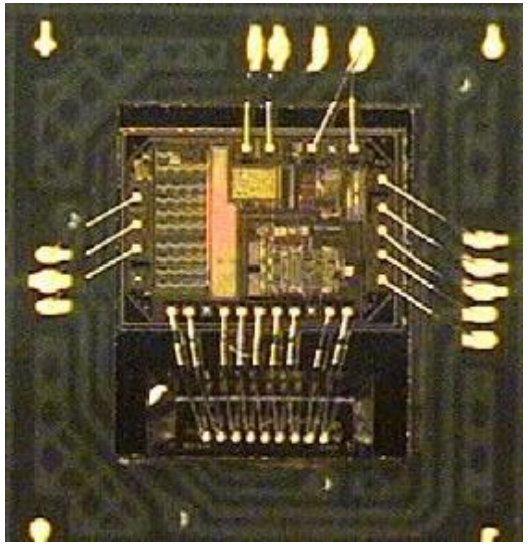
What’s inside our Accelerometers?

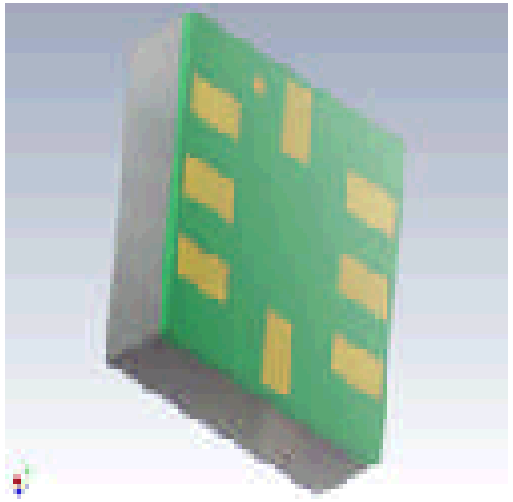




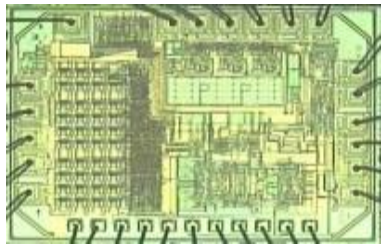
Mechanical Chip



Package
(shown without Plastic Mould)



Complete Package



Electrical Chip

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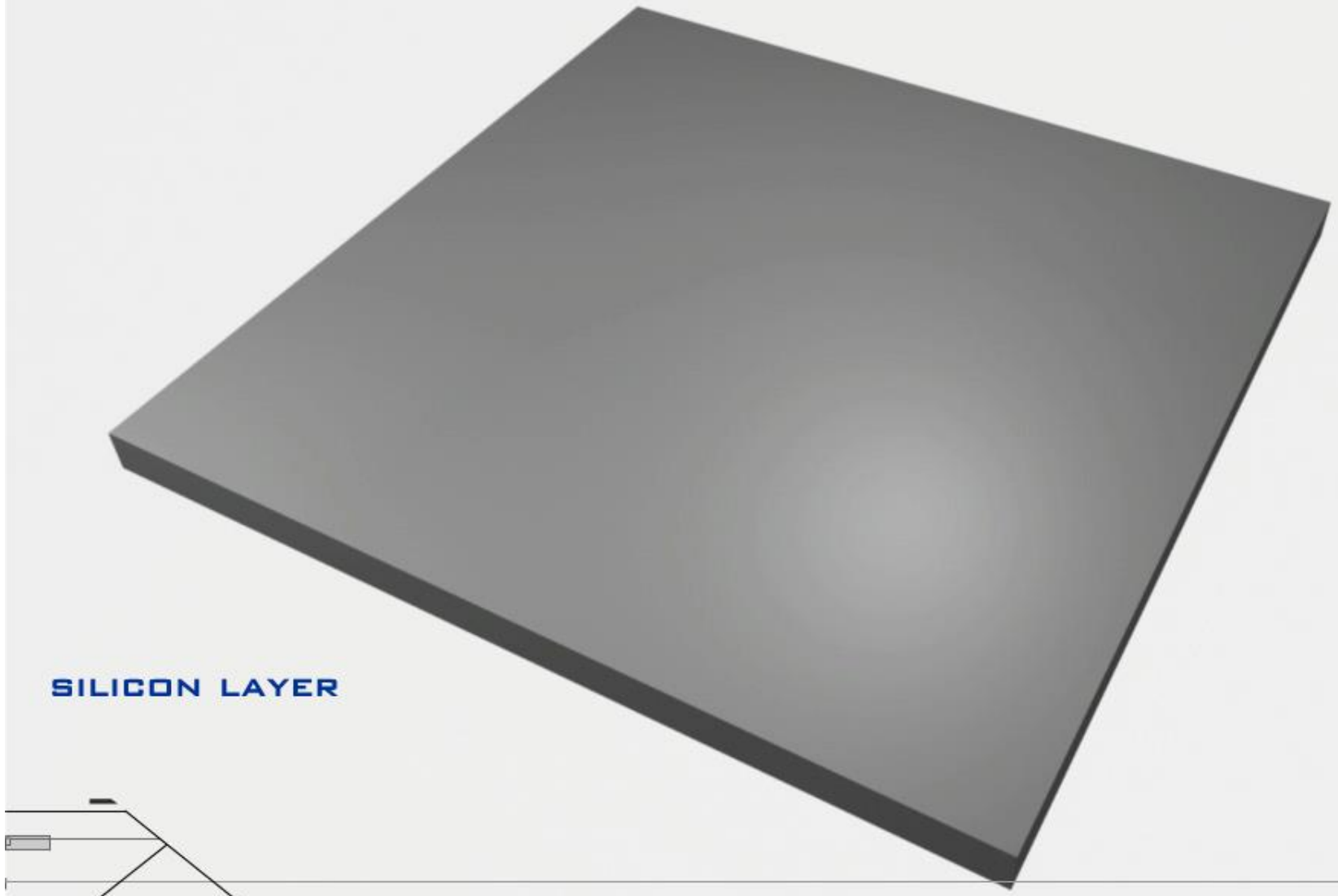
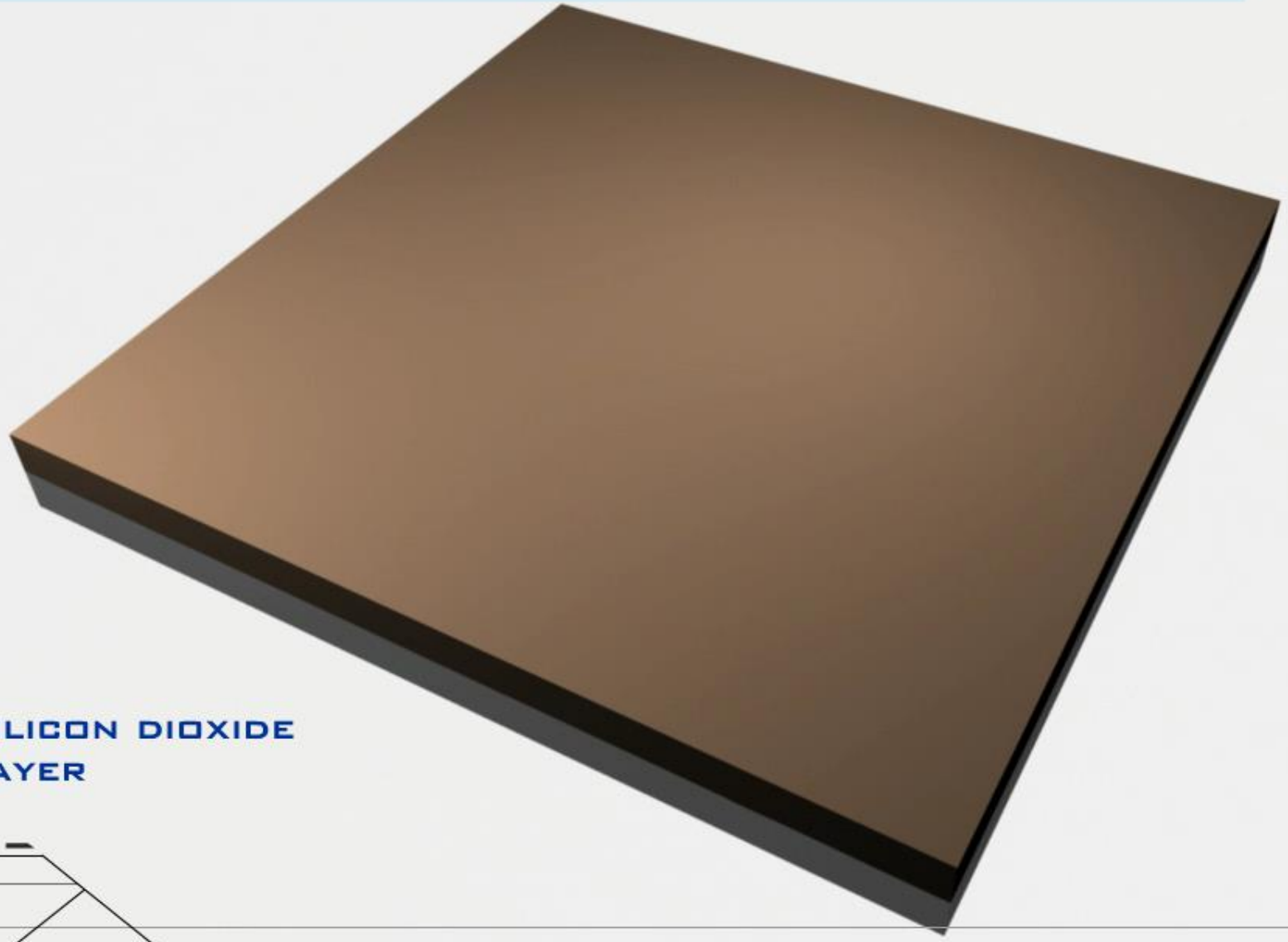
MEMS THELMA PROCESS



SILICON LAYER

MEMS THELMA PROCESS



SILICON DIOXIDE
LAYER

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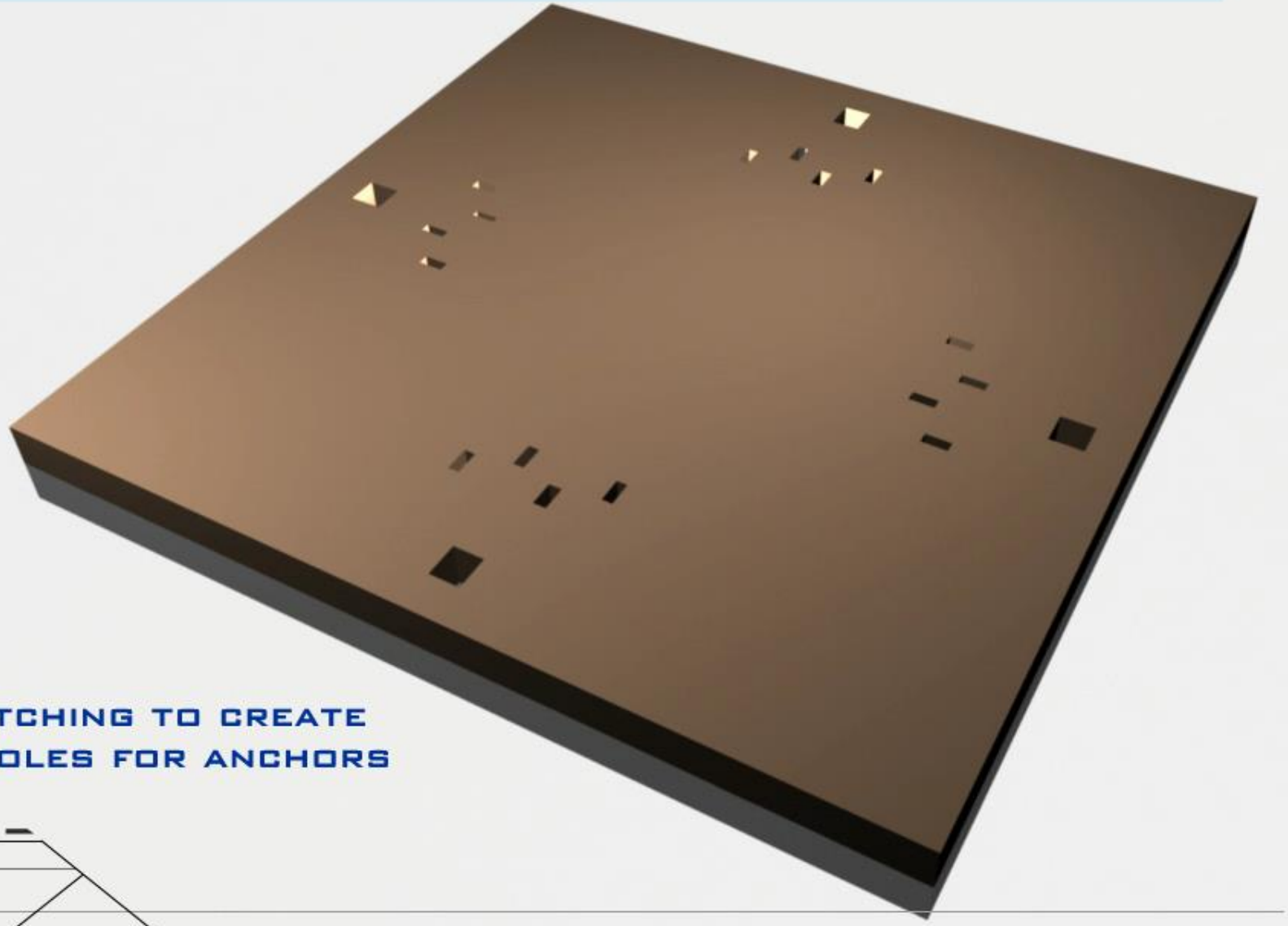
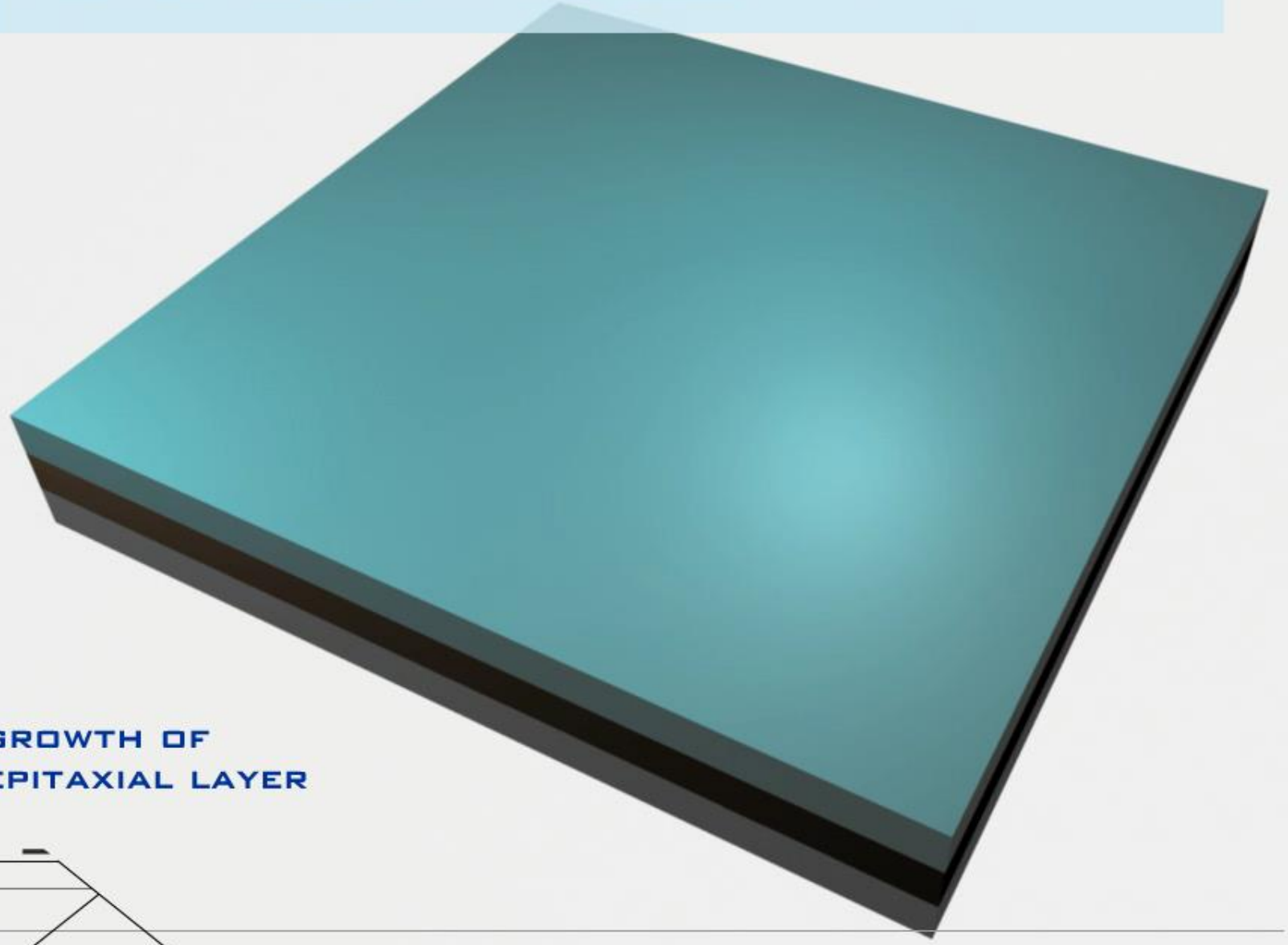
MEMS THELMA PROCESS



ETCHING TO CREATE
HOLES FOR ANCHORS

MEMS THELMA PROCESS



GROWTH OF
EPITAXIAL LAYER

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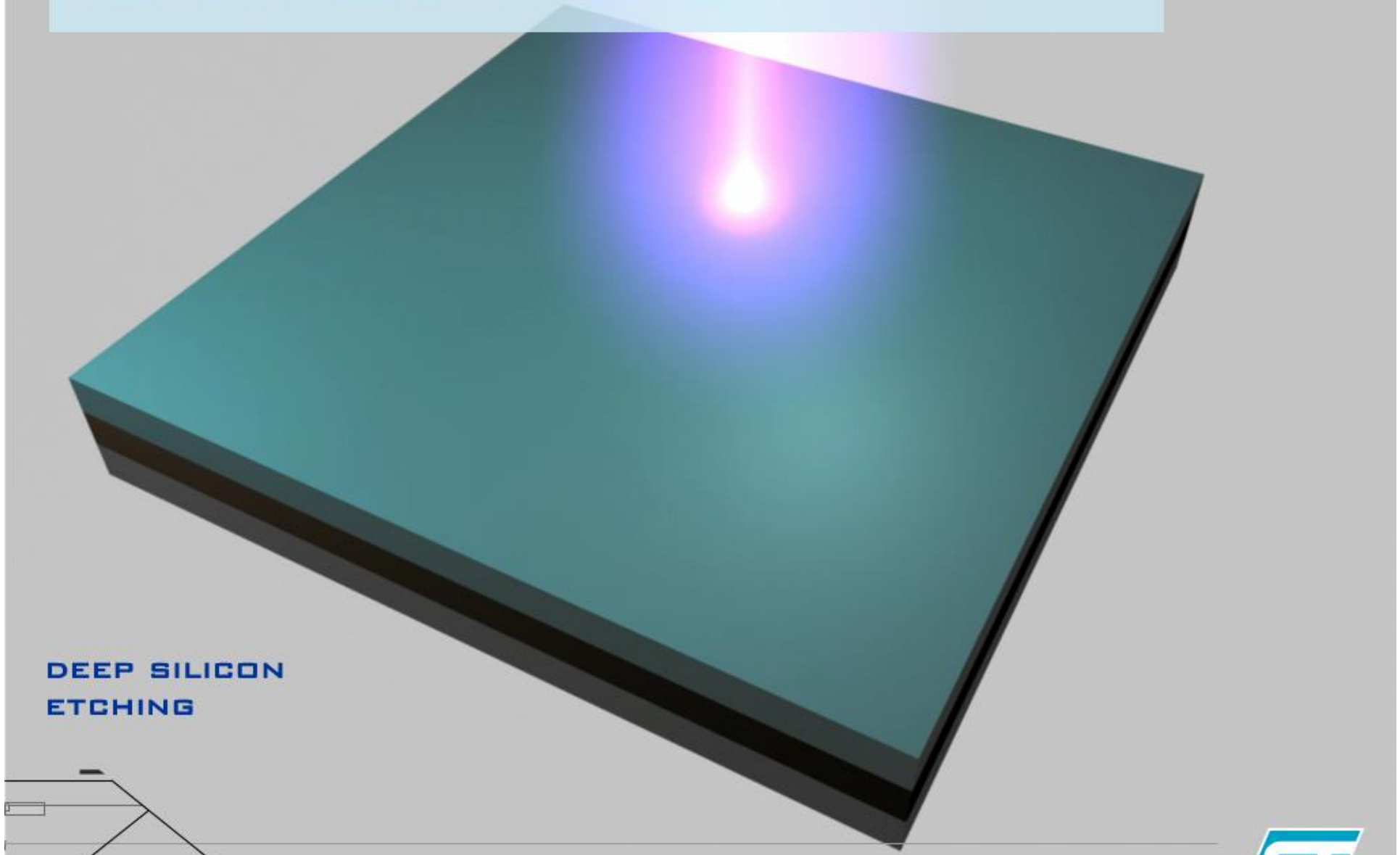
MEMS THELMA PROCESS



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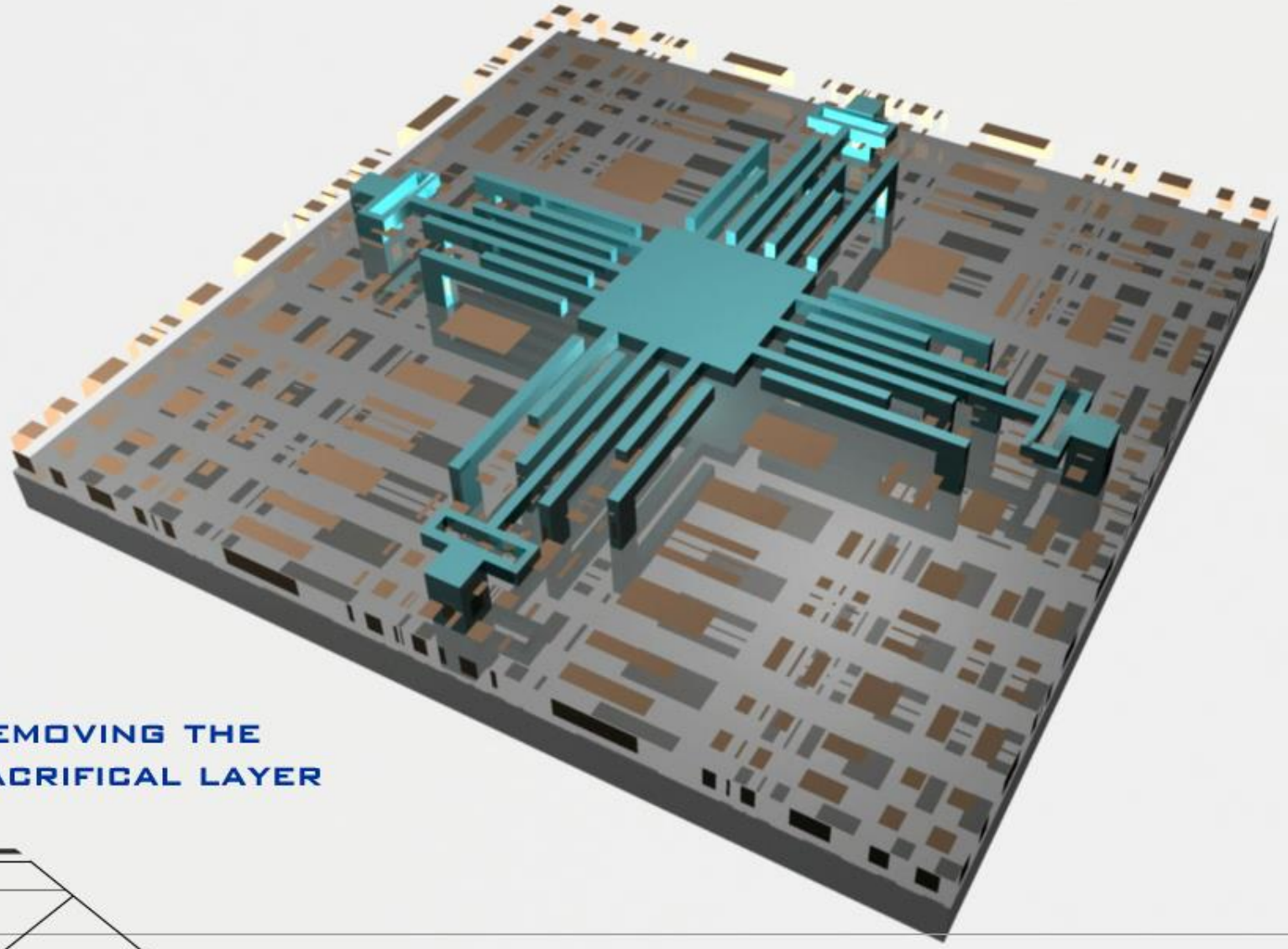
MEMS THELMA PROCESS



REMOVING THE SACRIFICAL LAYER

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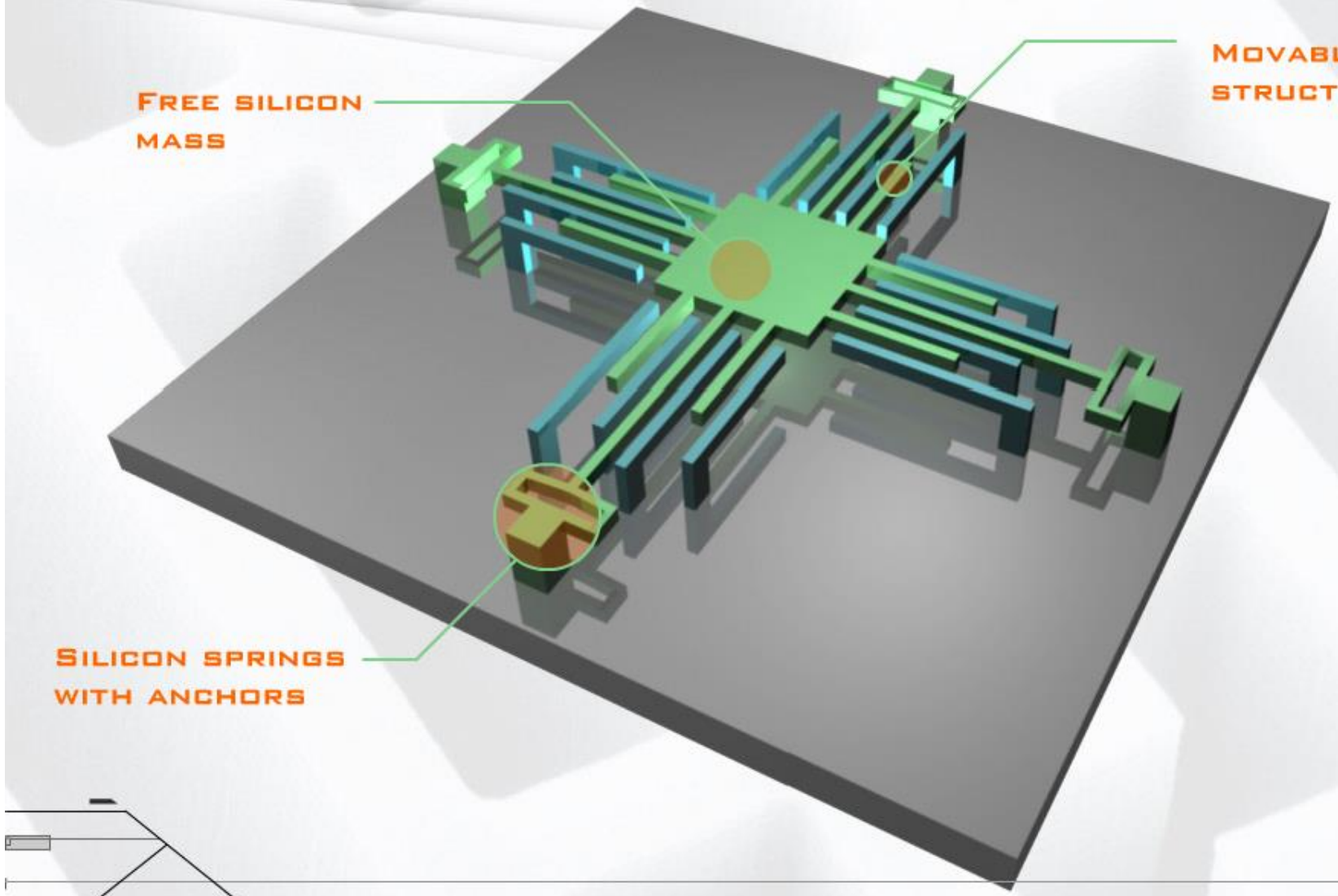
MEMS SENSOR MODEL



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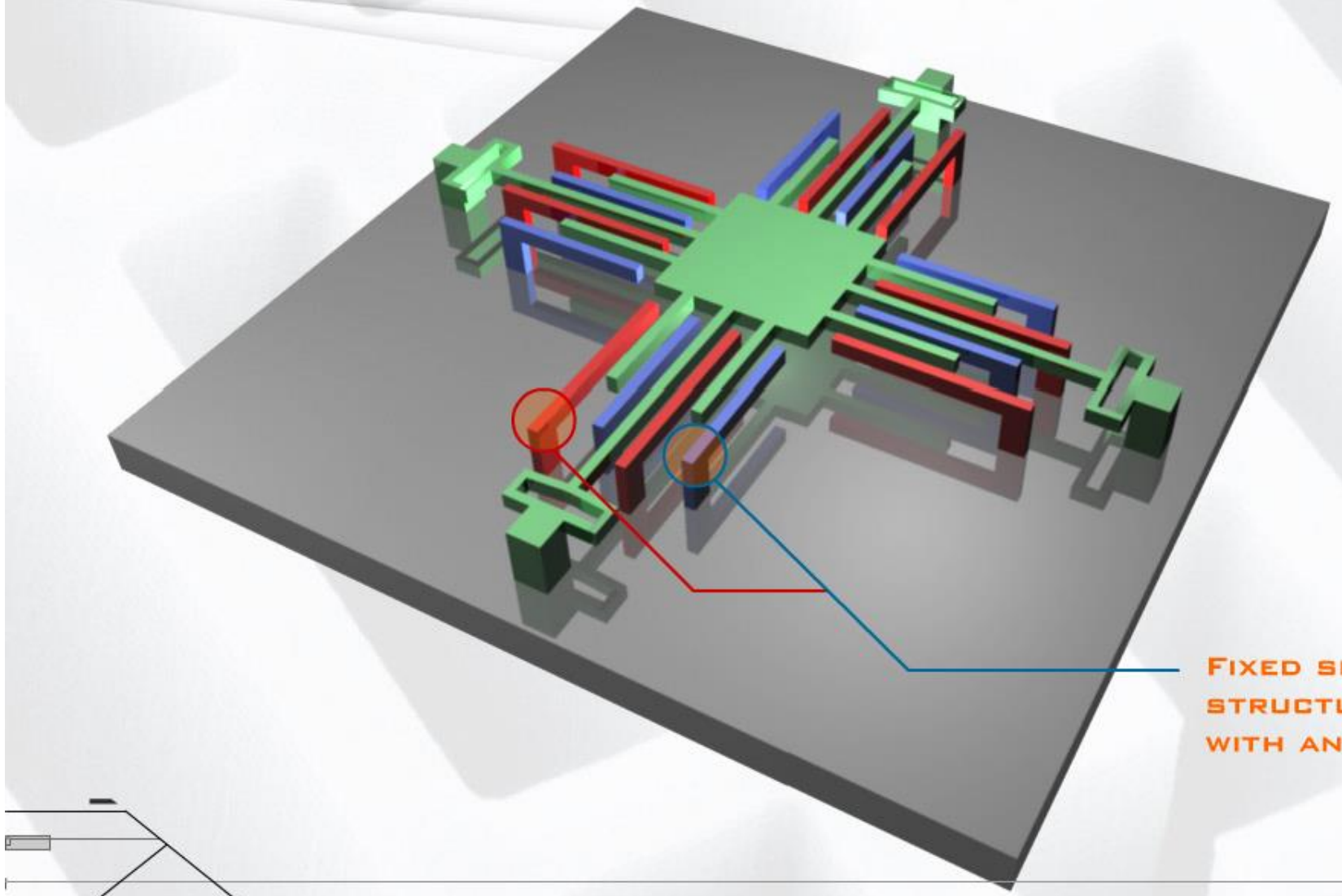
MEMS SENSOR MODEL



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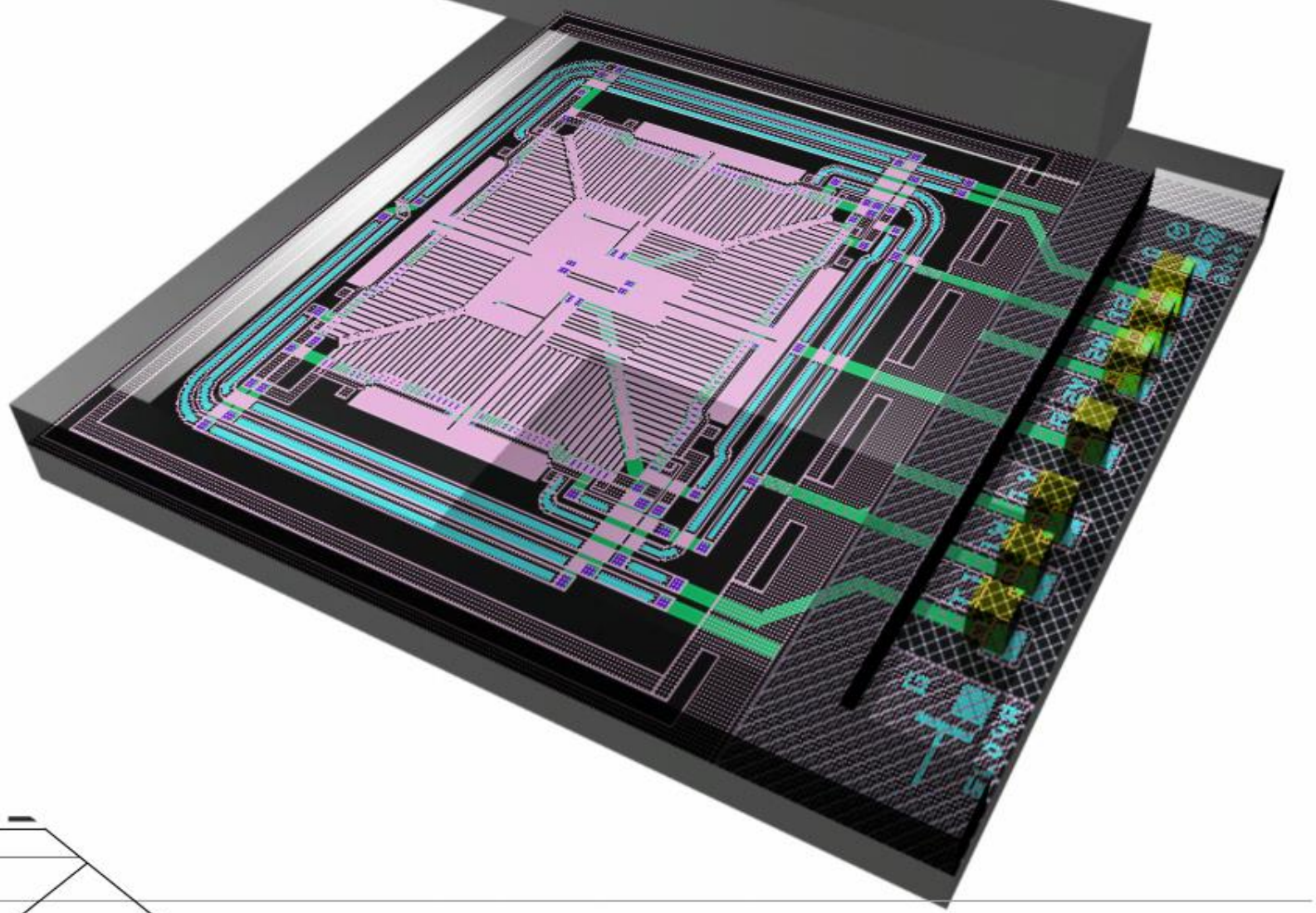
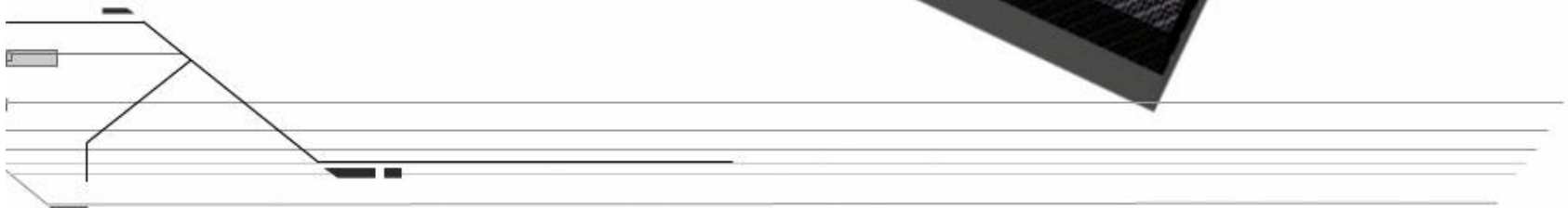
MEMS SILICON CAP





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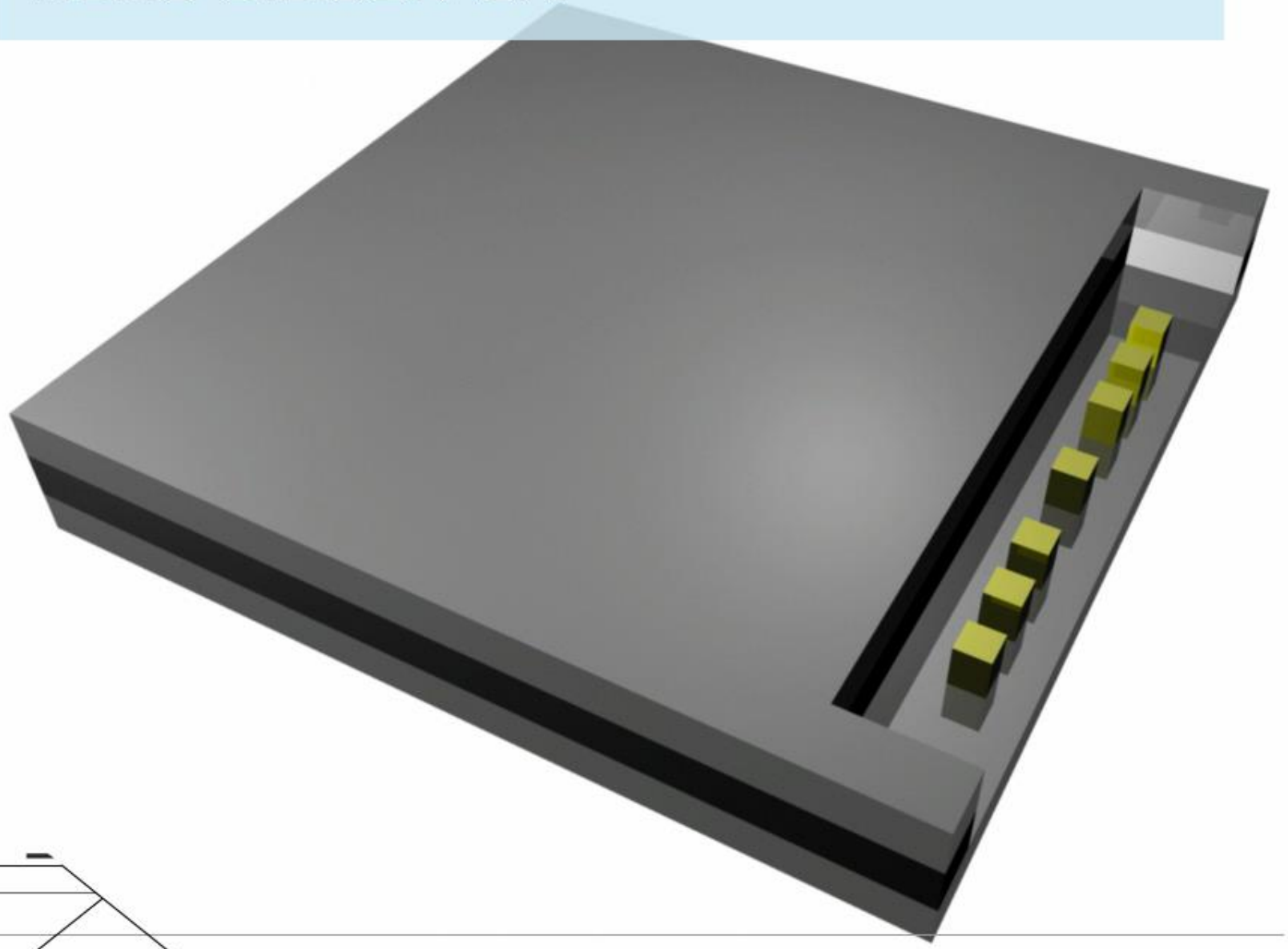
MEMS SILICON CAP



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Glossary

Glossary

Glossary of some of the terms used in this presentation

- **BGA**: Ball Grid Array
- **CBU**: Case per Billion Unit
- **CPA**: Corporate Package Automation
- **CSP**: Chip Size Package
- **MTBF**: Mean time between failure
- **MSL**: Moisture Sensitivity Level
- **OEE** = Overall Equipment Efficiency
- **PSSO**: Power Shrink Small Outline
- **PTM** : Packaging and Test Manufacturing
- **QFP**: Quad Flat Package
- **Recordable case**: Number of work-related injuries and illnesses per 100 employees
- **SMD**: Surface Mount Device
- **SO** : Small Outline
- **TUI** = Tester Utilization Index
- **WLCSP** : Wafer Level Chip Size Package

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